

Lab #2 Combinational Logic Design

Objective:

To introduce the design of some fundamental combinational logic building blocks.

Preparation:

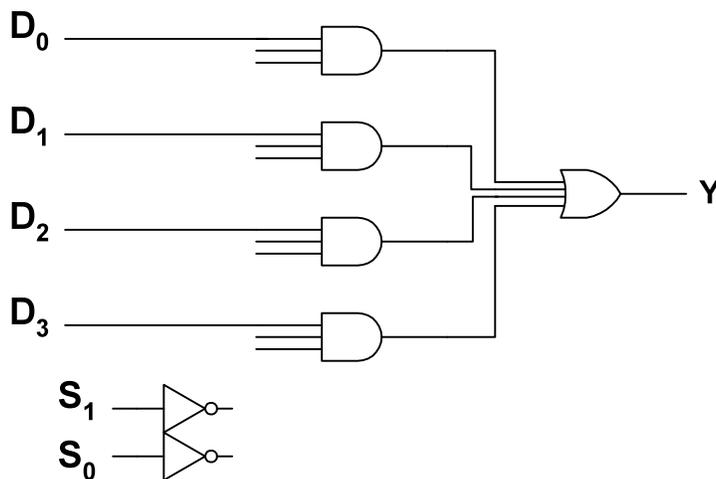
Read the following experiment and complete the circuits where required. Review sign-2's complement representations. Obtain the data sheets for each of the TTL devices below and bring a copy to your lab session.

Devices used:

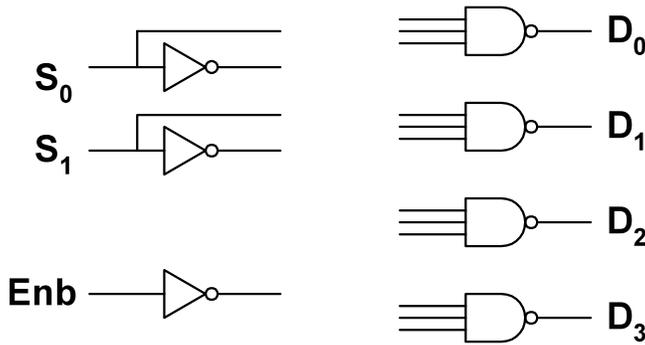
sn74LS00	2-input NAND	sn74LS86	Quad 2-input XOR
sn74LS10	Triple 3-input NAND	sn74LS138	3-to-8 line decoder
sn74LS20	Dual 4-input NAND	sn74LS283	4-bit binary adder
sn74LS47	BCD to 7-segment converter		

Experiment:

1. A multiplexer is a combinational circuit that selects binary information from one of several input sources and logically directs it to a single output channel. Complete the drawing of the circuit shown below to implement a single 4:1 MUX with inputs $D_0..D_3$, select lines S_0, S_1 and output Y . Build the circuit and verify its function table.

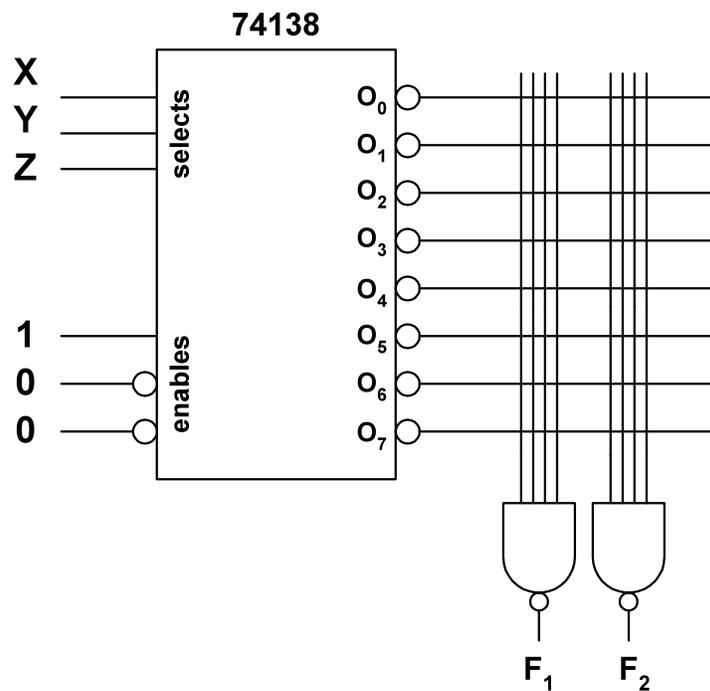


2. The n -bit binary decoder generates an output corresponding to each of the 2^n minterms of the input. Complete the drawing of the circuit shown below to implement a 2-to-4 line decoder with inputs S_0, S_1 , LO-true outputs $D_0..D_3$ and a single LO-true enable. Build the circuit and verify its function table.



3. Using switches for select and enable inputs and LEDs as outputs, verify the truth table for the 74138 3-to-8-line decoder. Carefully note its operation with regard to the enable inputs and the polarity of the outputs.

4. If the outputs of a decoder are considered as rows of a matrix and the column lines are provided by the inputs to NAND gates as shown in the figure below, we can view the generation of any logic functions F_1 and F_2 as a “programming” task. The “programming” is implemented as connections at the row/column intersections. Both F_1 and F_2 can be the summation of any 4 of the minterms of the input XYZ. Note that the number of outputs is restricted only by the number of NAND gates (two in this example) and that the number of minterms which may be summed is determined by the number of inputs to each NAND (four in this example).



Draw the truth table for a full adder, and “program” this circuit such that the output F_1 represents the sum S and output F_2 represents the carry C . Mark every intersection where there is a connection with an "X". Build the circuit and verify its operation.

5. An n-bit binary adder can be constructed as a chain of n full adders connected internally by the carry from one stage to the next. The input carry to the first full adder in the chain is C_0 and the output from the final stage is C_n . Since the input to C_0 has to propagate through all stages of the adder before it affects the output carry C_n , this device is sometimes called a *ripple carry adder*. This has the undesirable characteristic that the add time increases with n.

A better way is to form the sum and carry out as a logical combination of all the inputs to produce a fast parallel addition. An example is the sn74LS283 which is a 4-bit parallel adder with internal carry look-ahead logic.

Using switches and LEDs, verify the operation of the ‘283 device and complete the table below showing the decimal equivalent for the sum output Σ in both unsigned and sign-2’s complement.

C_0	A	B	Σ	Decimal Equivalent if Σ is unsigned	Decimal Equivalent if Σ is 2’s comp	C_4
0	0000	0000				
0	0000	0011				
0	0011	0000				
1	0011	0000				
0	0111	1000				
1	0111	1000				
0	1000	1000				
0	0011	1111				
0	0111	1111				
0	1001	1111				
0	1111	1111				
1	1111	1111				

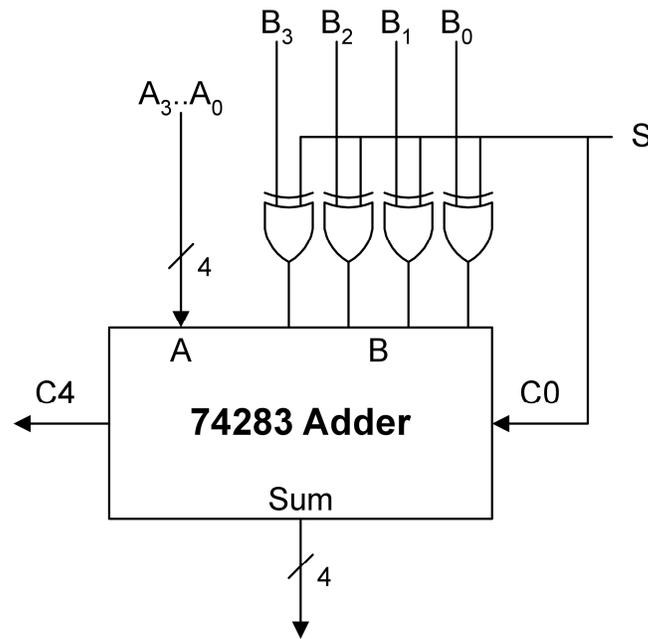
Using the digital ‘scope, devise a way to measure the propagation delay from application of a C_0 input to the appearance of a C_4 output.

Measured Propagation delay of Carry : _____

Propagation delay from spec sheets: **Min:** _____ **Max:** _____

6. The parallel adder may be used in the following circuit to add or subtract 4-bit numbers under control of input S.

When $S=0$, the output is $A + B$. When $S=1$, the output is $A - B$. Explain why this is so. Construct this circuit and verify its proper operation.

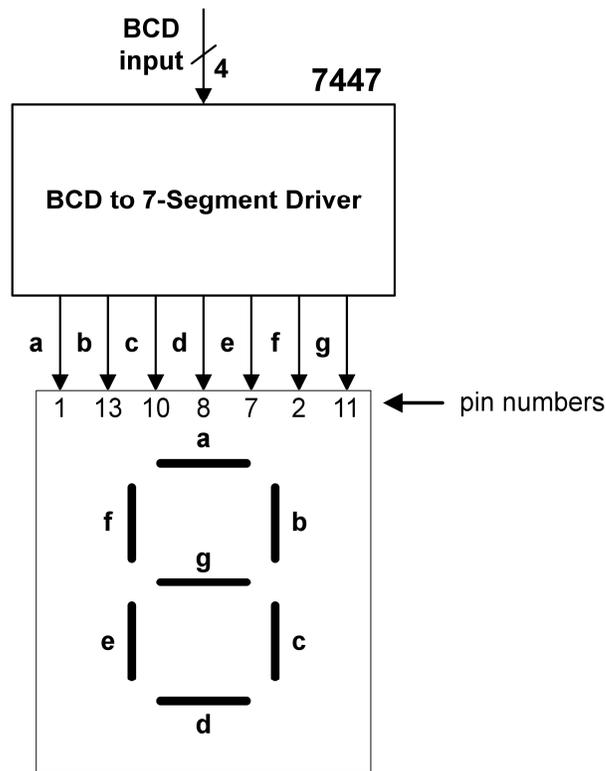


The adder/subtractor may be used to take the 2's complement of an input number B by setting $A=0000$ and $S=1$. Try this for several values. In the last circuit, we use this feature to take the 2's complement of a number if it is negative in order to provide input to a display.

Note: Leave this circuit connected; it will be used in the last part of this lab.

7. Seven-segment displays are ubiquitous. Each segment can be activated by pulling its corresponding output LO. One way of driving the display is by way of an sn74LS47 BCD to 7-segment converter which contains the proper current-limiting capability. Connect the circuit as shown below and verify its proper operation for all 16 input combinations. Note that only BCD digits 0 to 9 produce a valid display.

Note: *Never* connect the inputs of the display directly to ground or +5v. This will permanently damage the display !



Note: *Leave this circuit connected; it will be used later in this lab.*

8. Now, connect the output of the adder/subtractor circuit in part 6 to the BCD inputs of the circuit of part 7. Set $A = 0000$, $S = B_3$ and test the circuit. The display should show the absolute value of the sign-2's complement input set on B.